

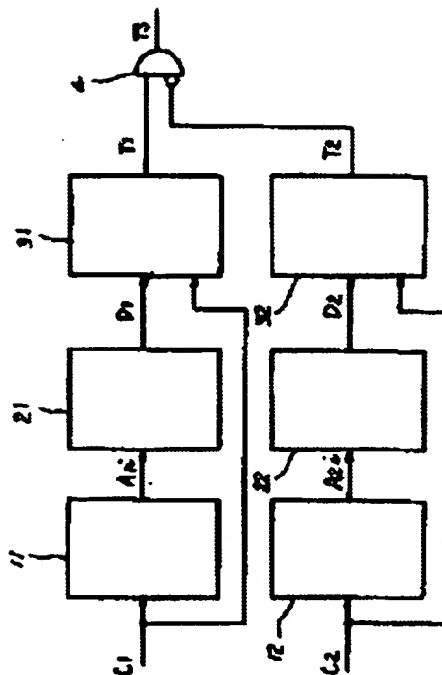
**TIMING FORMATION CIRCUIT**

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**Abstract of JP56068813**

**PURPOSE:** To produce a timing pulse having a higher resolution than the cycle of the working block, by using several units of the timing formation circuit consisting of the counter circuit, ROM and D type FF.

**CONSTITUTION:** The two sets of the timing formation circuits are constituted with the counter circuits 11 and 12, ROMs 21 and 22 plus D type FFs 31 and 32. The working clocks C1 and C2 of each timing formation circuit are set with a delay with every cycle  $tO$  of the basic clock, and at the same time the outputs T1 and T2 of each timing formation circuit are given to the combination logic circuit 4. In such formation of the circuit, the timing pulse having the resolution  $tO$  can be produced through a unit of the timing formation circuit although only the timing pulse of resolution  $2tO$  is so far produced.



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